



Newsletter

III-N compound semiconductors New Patent Applications

January 2011

**Information**

This monthly newsletter provides you with an overview on new patent applications in the III-N compound semiconductors area.

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CONTENTS

Ion sensitive field effect transistor and production method thereof.....	3
Nitride semiconductor device.....	3
High performance power switch	4
Enhancement mode hemt for digital and analog applications	4
Group III nitride semiconductor optical element and epitaxial substrate	5
Nitride-based semiconductor light-emitting element.....	5
Nitride-based semiconductor light-emitting element.....	6
Manufacturing method for semiconductor device.....	6
Method for fabricating flip chip gallium nitride light emitting diode.....	7
Gallium nitride-based semiconductor laser diode.....	7
Nitride-based semiconductor light emitting device.....	8
Method for manufacturing nitride semiconductor substrate	8
Composite substrate with crystalline seed layer and carrier layer with a coincident cleavage plane .	9
Fabrication method of gallium nitride-based compound semiconductor.....	9
Nitride semiconductor chip, method of fabrication thereof, and semiconductor device	9

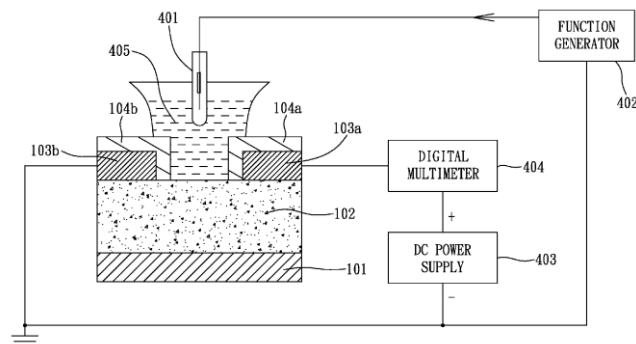


Ion sensitive field effect transistor and production method thereof

Applicant(s): Not available

Patent number: US2011018038

Abstract: The present invention discloses an ion sensitive field effect transistor, comprising: a GaN/sapphire layer, used as a substrate an a-InN:Mg epilayer, deposited on the GaN/sapphire layer, used to provide a current path a first metal contact, deposited on the a-InN:Mg epilayer to provide drain contact and a second metal contact, deposited on the a-InN:Mg epilayer to provide source contact and a patterned insulating layer, used to cover the first metal contact, the second metal contact and the a-InN:Mg epilayer, wherein the patterned insulating layer has a contact window defining an exposure area of the a-InN:Mg epilayer.



Nitride semiconductor device

Applicant(s): Panasonic Corp

Patent number: WO2011010419

Abstract: Disclosed is a nitride semiconductor device achieving both low on-resistance and high withstand voltage using an InAlN/AlGaIn material. The nitride semiconductor device is provided with: a hetero structural layer (10) wherein an InAlN layer (104) composed of $\text{In}_a\text{Al}_b\text{Ga}_c\text{N}_{1-a-b-c}$ ($1 > a > 0$, $1 > b > 0$, $1 > c = 0$), which has a band gap (E_{g1}) and a lattice constant difference of less than 0.3% compared with the lattice constant of GaN, and a GaN layer (103) composed of $\text{In}_d\text{Al}_e\text{Ga}_f\text{N}_{1-d-e-f}$ ($1 > d = 0$, $1 > e = 0$, $1 = f > 0$) having a band gap (E_{g2}) ($E_{g1} > E_{g2}$) are sequentially laminated a Schottky electrode (109), which is formed on the first side surface of the hetero structural layer such that the electrode is in contact with the hetero interface of the hetero structural layer, and which is Schottky-connected with the hetero structural layer and an ohmic electrode (110), which is formed on the second side surface of the hetero structural layer, said second side surface being different from the first side surface, such that the electrode is in contact with the hetero interface of the hetero structural layer, and which is in ohmic contact with the hetero structural layer.

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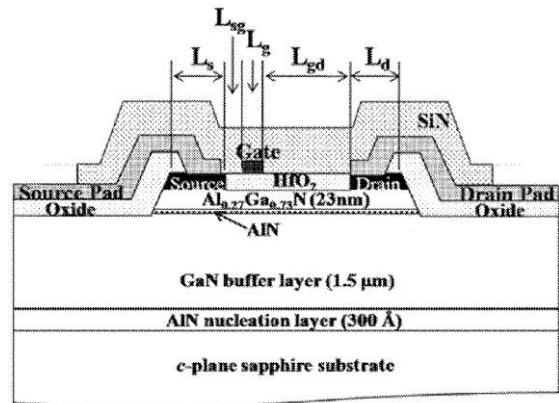


High performance power switch

Applicant(s): Univ Cornell

Patent number: WO2011008665

Abstract: In one example, we describe a new high performance AlGa_{0.27}Ga_{0.73}N metal-insulator-semiconductor hetero structure field-effect transistor (MISHFET), which was fabricated using HfO₂ as the surface passivation and gate insulator. The gate and drain leakage currents are drastically reduced to tens of nA, before breakdown. Without field plates, for 10[μm]m of gate-drain spacing, the off-state breakdown voltage is 1035V with a specific on-resistance of 0.9mΩ-cm². In addition, there is no current slump observed from the pulse measurements. This is the best performance reported on GaN-based, fast power-switching devices on sapphire, up to now, which efficiently combines excellent device forward, reverse, and switching characteristics. Other variations, features, and examples are also mentioned here.

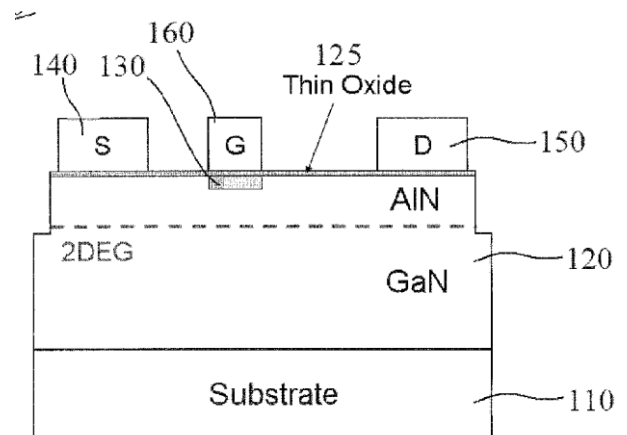


Enhancement mode hemt for digital and analog applications

Applicant(s): Univ Florida

Patent number: WO2011008531

Abstract: An enhancement mode (E-mode) HEMT is provided that can be used for analog and digital applications. In a specific embodiment, the HEMT can be an AlN/GaN HEMT. The subject E-mode device can be applied to high power, high voltage, high temperature applications, including but not limited to telecommunications, switches, hybrid electric vehicles, power flow control and remote sensing. According to an embodiment of the present invention, E-mode devices can be fabricated by performing an oxygen plasma treatment with respect to the gate area of the HEMT. The oxygen plasma treatment can be, for example, an O₂ plasma treatment. In addition, the threshold voltage of the E-mode HEMT can be controlled by adjusting the oxygen plasma exposure time. By using a masking layer protecting regions for depletion mode (D-mode) devices, D-mode and E-mode devices can be fabricated on a same chip.



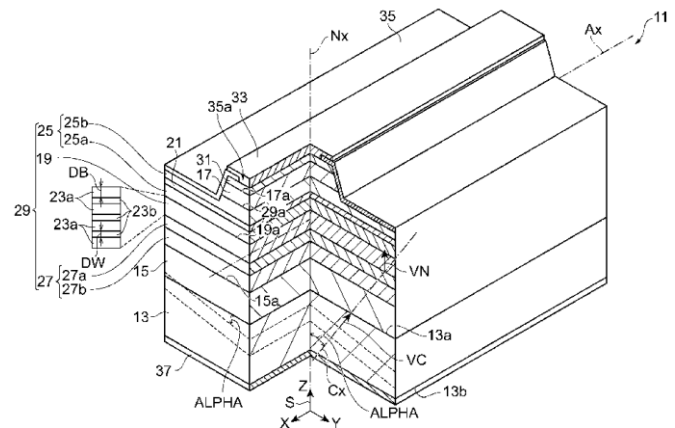


Group III nitride semiconductor optical element and epitaxial substrate

Applicant(s): Sumitomo Electric Industries

Patent number: WO2011007777

Abstract: Provided is a group III nitride-based semiconductor optical element including a p-type GaN-based semiconductor layer that has been made to exhibit low electrical resistance. A main surface (13a) of a supporting body (13) forms an angle (ALPHA) that is at least 40 degrees and at most 140 degrees relative to a reference plane (Sc), and the reference plane (Sc) is perpendicular to a reference axis (Cx) extending along a c axis of the group III nitride-based semiconductor. The main surface (13a) exhibits either semi-polarity or non-polarity. An n-type GaN-based semiconductor layer (15) is provided on the main surface (13a) of the supporting body (13). The n-type GaN-based semiconductor layer (15), an active layer (19), and the p-type GaN-based semiconductor layer (17) are arranged along a normal axis (Nx). In the p-type GaN-based semiconductor layer (17), magnesium is added as a p-type dopant, and the p-type GaN-based semiconductor layer (17) includes carbon as a p-type dopant. Carbon concentration of the p-type GaN-based semiconductor layer (17) is at least $2 \times 10^{16} \text{ cm}^{-3}$ and at most $1 \times 10^{19} \text{ cm}^{-3}$.

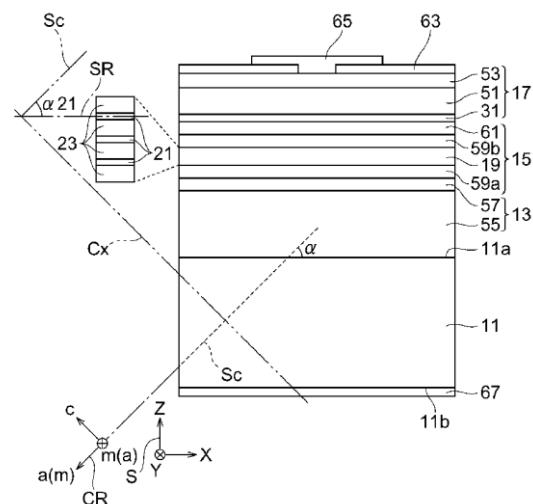


Nitride-based semiconductor light-emitting element

Applicant(s): Sumitomo Electric Industries

Patent number: WO2011007641

Abstract: A nitride-based semiconductor light-emitting element (LE1, LD1) is characterized by being provided with a gallium nitride substrate (11) having a principal surface (11a) that forms an angle (a) in the range of 40 DEG -50 DEG (both inclusive) and 90 DEG (exclusive)-130 DEG (inclusive) with a reference plane (Sc) orthogonal to a reference axis (Cx) extending in a c-axis direction, an n-type gallium nitride-based semiconductor layer (13), a second gallium nitride-based semiconductor region (17), and a light-emitting layer (15) including a plurality of well layers (21) each produced from InGaN and a plurality of barrier layers (23) each produced from a GaN-based semiconductor, wherein the direction of piezoelectric polarization of the plurality of well layers (21) is a direction from the n-type gallium nitride-based semiconductor layer (13) to the second gallium nitride-based semiconductor region (17).



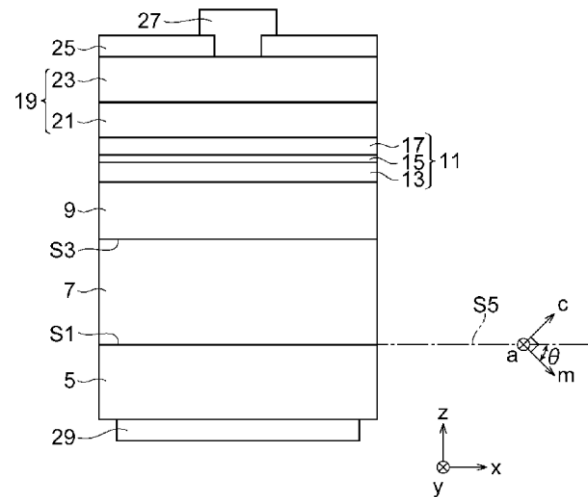


Nitride-based semiconductor light-emitting element

Applicant(s): Sumitomo Electric Industries

Patent number: WO2011007637

Abstract: Provided is a nitride-based semiconductor light-emitting element having improved carrier injection efficiency into the well layer. The element comprises a substrate (5) formed from a hexagonal-crystal gallium nitride semiconductor an n-type gallium nitride semiconductor region (7) disposed on a main surface (S1) of the substrate (5) a light-emitting layer (11) having a single quantum well structure disposed on the n-type gallium nitride semiconductor region (7) and a p-type gallium nitride semiconductor region (19) disposed on the light-emitting layer (11). The light-emitting layer (11) is disposed between the n-type gallium nitride semiconductor region (7) and the p-type gallium nitride semiconductor region (19). The light-emitting layer (11) comprises a well layer (15), a barrier layer (13), and a barrier layer (17). The well layer (15) is InGaN. The main surface (S1) extends, from a surface perpendicular to the c axial direction of the hexagonal-crystal gallium nitride semiconductor, along a reference plane (S5) inclined at an angle of inclination within a range between 63 and 80 or between 100 and 117.

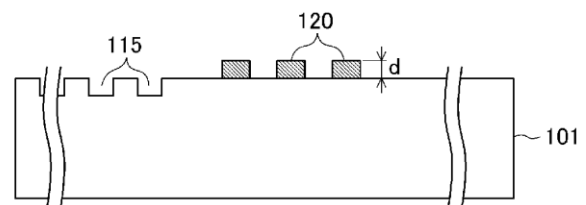


Manufacturing method for semiconductor device

Applicant(s): Panasonic Corp

Patent number: WO2011007472

Abstract: Upon a substrate (101) comprising materials that are transparent to light sources for detecting alignment marks, second alignment marks (120) comprising materials that have a different refractive index than said substrate (101) are formed. A GaN epitaxial layer comprising an active layer (105) is subsequently grown upon the substrate (101) in a manner embedding the second alignment marks (120). An exposure is thereafter aligned with the GaN epitaxial layer while referencing the second alignment marks (120).



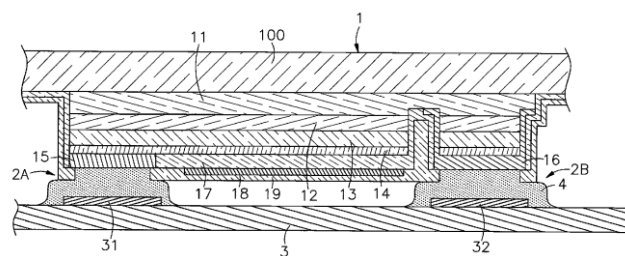


Method for fabricating flip chip gallium nitride light emitting diode

Applicant(s): Not available

Patent number: US2011014734

Abstract: The present invention discloses a method for fabricating a flip chip GaN LED, which has a predetermined region on an epitaxial layer for forming a first groove to expose a portion of the substrate, and another predetermined region on the epitaxial layer for forming a second groove to expose a portion of N type GaN Ohm contacting layer. On a side of the first groove, there are a translucent conducting layer, an N type electrode pad, a first isolation protection layer, a metallic reflection layer and a second isolation protection layer sequentially formed on the surface of a P type GaN Ohm contacting layer. On another side of the first groove, a translucent conducting layer, an N type electrode pad, a first isolation protection layer and a second isolation protection layer are sequentially formed on the surface of an N type GaN Ohm contacting layer. The above structure not only can provide a flat surface for electrical connection of the P type and N type electrode pads with the circuit board, but also to keep the metallic reflection layer from conducting electricity to avoid increasing the forward voltage and the power consumption, and accordingly to promote the light emitting performance of the LED.

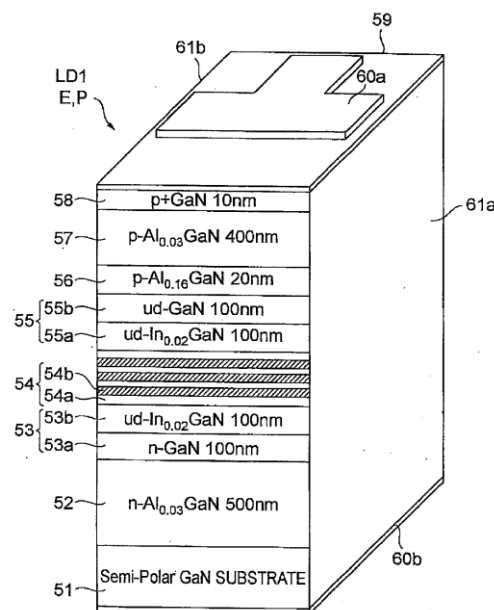


Gallium nitride-based semiconductor laser diode

Applicant(s): Sumitomo Electric Industries

Patent number: US2011013657

Abstract: Provided is a III-nitride semiconductor laser diode capable of lasing to emit light of not less than 500 nm with use of a semipolar plane. Since an active layer 29 is provided so as to generate light at the wavelength of not less than 500 nm, the wavelength of light to be confined into a core semiconductor region 19 is a long wavelength. A first optical guide layer 27 is provided with a two-layer structure, and a second optical guide layer 31 is provided with a two-layer structure. A material of a cladding layer 21 comprised of at least either of AlGaIn and InAlGaIn is different from the III-nitride semiconductor, and the thickness D15 of a first epitaxial semiconductor region 15 is larger than the thickness D19 of the core semiconductor region 19 however, the misfit dislocation densities at first to third interfaces J1, J2 and J3 are not more than 1106 cm^{-1} , thereby preventing lattice relaxation from occurring in the semiconductor layers at these interfaces J1, J2 and J3 because of the c-plane that acts as a slip plane.



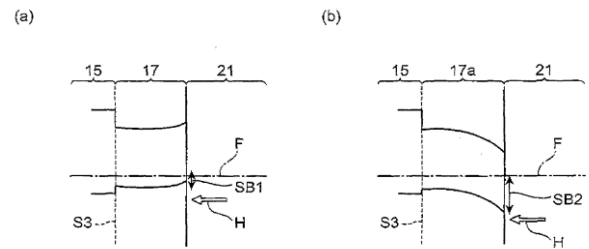


Nitride-based semiconductor light emitting device

Applicant(s): Sumitomo Electric Industries

Patent number: EP2276079

Abstract: An object is to provide a nitride-based semiconductor light emitting device capable of preventing a Schottky barrier from being formed at an interface between a contact layer and an electrode. LD 1 is provided as a nitride-based semiconductor light emitting device provided with a GaN substrate 3, a hexagonal GaN-based semiconductor region 5 provided on a primary surface S1 of the GaN substrate 3 and including a light emitting layer 11, and a p-electrode 21 provided on the GaN-based semiconductor region 5 and comprised of metal. The GaN-based semiconductor region 5 includes a contact layer 17 involving strain, the contact layer 17 is in contact with the p-electrode, the primary surface S1 extends along a reference plane S5 inclined at a predetermined inclination angle from a plane perpendicular to the c-axis direction of the GaN substrate 3, and the inclination angle is either in the range of more than 40 DEG and less than 90 DEG or in the range of not less than 150 DEG and less than 180 DEG. The GaN-based semiconductor region 5 is lattice-matched with the GaN substrate 3.

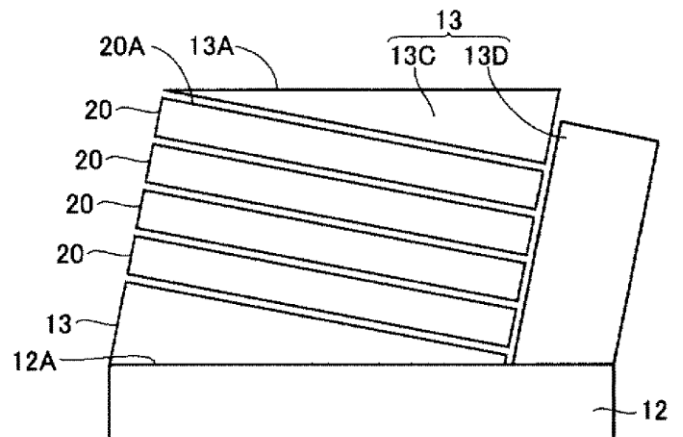


Method for manufacturing nitride semiconductor substrate

Applicant(s): Sumitomo Electric Industries

Patent number: WO2011004726

Abstract: Disclosed is a method for manufacturing a nitride semiconductor substrate, which is capable of suppressing polycrystalline growth and efficiently manufacturing the nitride semiconductor substrate having a nonpolar plane as a main surface. Specifically disclosed is a method for manufacturing a GaN substrate that is a nitride semiconductor substrate, the method being provided with a step (S10, S20) for preparing a base substrate produced from GaN and having a main surface with an off angle of 4.1 DEG -47.8 DEG with respect to the [1-100] plane, a step (S40) for epitaxially growing a semiconductor layer produced from GaN on the main surface of the base substrate, and a step (S50) for obtaining the GaN substrate having the m plane as a main surface from the semiconductor layer.



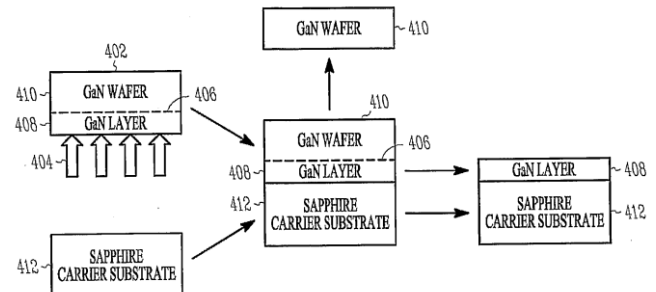


Composite substrate with crystalline seed layer and carrier layer with a coincident cleavage plane

Applicant(s): Soitec Silicon On Insulator

Patent number: WO2011004211

Abstract: A structure and a method can provide forming a structure for a crystalline seed layer material, such as GaN, on a crystalline carrier material, such as sapphire, aligned such that a common crystal plane exists between the two materials. The common crystal plane may provide for a fracture surface along a cleavage plane that may be oriented to be perpendicular to the top surface of an optoelectronic device as well as perpendicular to a light emission direction.

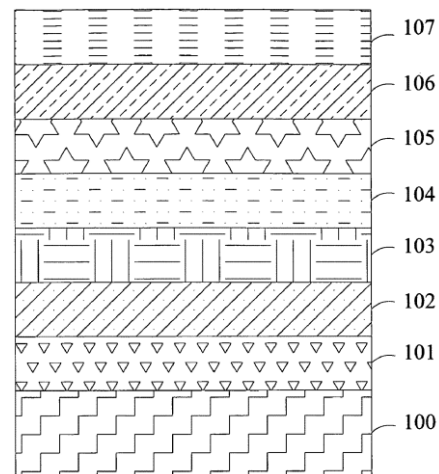


Fabrication method of gallium nitride-based compound semiconductor

Applicant(s): Sino American Silicon Products Inc

Patent number: US2011003420

Abstract: The present invention discloses a method for fabricating gallium nitride(GaN)-based compound semiconductors. Particularly, this invention relates to a method of forming a transition layer on a zinc oxide (ZnO)-based semiconductor layer by the steps of forming a wetting layer and making the wetting layer nitridation. The method not only provides a function of protecting the ZnO-based semiconductor layer, but also uses the transition layer as a buffer layer for a following epitaxial growth of a GaN-based semiconductor layer, and thus, the invention may improve the crystal quality of the GaN-based semiconductor layer effectively.

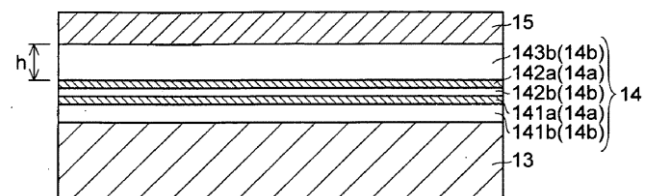


Nitride semiconductor chip, method of fabrication thereof, and semiconductor device

Applicant(s): Sharp Kk

Patent number: US2011001126

Abstract: A nitride semiconductor chip is provided that offers enhanced luminous efficacy and an increased yield as a result of an improved EL emission pattern and improved surface morphology (flatness). This nitride semiconductor laser chip (nitride semiconductor chip) includes a GaN substrate having a principal growth plane and individual nitride semiconductor layers formed on the principal growth plane of the GaN substrate. The principal growth plane is a plane having an off angle in the a-axis direction relative to the m plane, and the individual nitride semiconductor layers include a lower clad layer of AlGaIn. This lower clad layer is formed in contact with the principal growth plane of the GaN substrate.





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